INTERNATIONAL MICROCIRCUITS INC

CMOS LSI
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

T-50-17

PRODUCT FEATURES

- General Purpose Applications: CATV, AM/FM Radios, Scanning Receivers, 2-Way Radios, Amateur Radios, TV Tuning
- >30 MHz Typical Input Capability @ V_{DD} = 5V
- On- or Off-Chip Reference Oscillator Operation with Buffered Output
- Compatible with the SPI (Serial Peripheral Interface) on CMOS MCU's
- Lock Detect Signal
- Two Open-Drain Switch Outputs
- Single Modulus/Serial Programming
- 8 User-Selectable ÷R Values: 16, 512, 1024, 2048, 3668, 4096, 6144, 8192
- ÷N Range = 3 to 16383
- Linearized Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single-Ended (3-State), Double-Ended
- Packaging Options Include: Plastic and Ceramic Dual-In-Line, Plastic J-Leaded, and Ceramic Leadless Chip Carriers, and Small-Outline Packages. Die are available for Hybrid Applications.
- Grades Available Include: Commercial, Military Operating Range, and Military Screened

PRODUCT DESCRIPTION

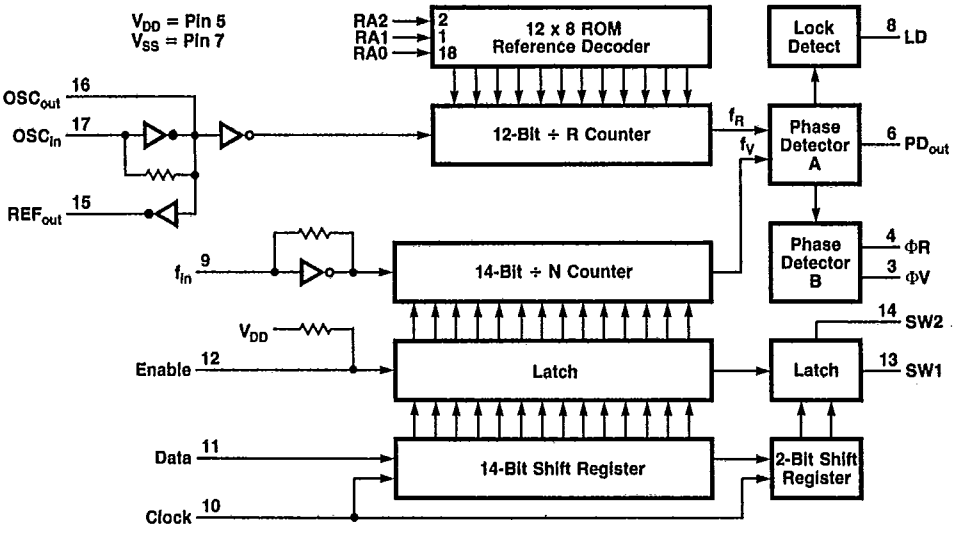
The IMI145155 is one of a family of LSI PLL frequency synthesizers from International Microcircuits. In the 18-pin ceramic or plastic dual-in-line packages, this product is pin-for-pin compatible with the MC145155, and can be used as a direct replacement with identical or superior operating characteristics. This product can be alternatively packaged to meet your needs. MIL-STD-883 screening is available for high-reliability applications.

The IMI145155 is programmed by a clocked, serial input 16-bit data stream. The device features a reference oscillator, selectable-reference divider, digital-phase detector, 14-bit programmable ÷N counter, and the necessary shift register and latch circuitry for accepting the serial input data. When combined with a loop filter and VCO, the IMI145155 can provide all the remaining functions for a PLL frequency synthesizer operating to the device's frequency limit. For higher VCO frequency operation, a down mixer or a fixed divide prescaler can be used between the VCO and the IMI145155.

The IMI145155, IMI145156, IMI145157, and IMI145158 CMOS PLL frequency synthesizers have serial programmable inputs with a single or dual modulus capability, transmit/receive offsets, selection of phase detector type, and choice of reference divider integer values.

If your application requires additional features, please contact our factory. Our engineers can quickly design a product to meet your requirements.

BLOCK DIAGRAM



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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +10	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} +0.5	Vdc
Operating Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

(Voltage Referenced to V_{SS})

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	−55°C		−40°C		25°C			85°C		125°C		Units
			Min	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Max	
Power Supply Voltage	V_{DD}	—	3	8	3	8	3	—	8	3	8	3	8	Vdc
Output Voltage V_{in} = V_{DD} or 0	V_{OL}	3	—	0.05	—	0.05	—	0	0.05	—	0.05	—	0.05	Vdc
		5	—	0.05	—	0.05	—	0	0.05	—	0.05	—	0.05	
		8	—	0.05	—	0.05	—	0	0.05	—	0.05	—	0.05	
V_{in} = 0 or V_{DD}	V_{OH}	3	2.95	—	2.95	—	2.95	3	—	2.95	—	2.95	—	
		5	4.95	—	4.95	—	4.95	5	—	4.95	—	4.95	—	
		8	7.95	—	7.95	—	7.95	8	—	7.95	—	7.95	—	
Input Voltage V_O = 2.5 or 0.5	V_{IL}	3	—	0.9	—	0.9	—	1.35	0.9	—	0.9	—	0.9	Vdc
V_O = 4.5 or 0.5		5	—	1.5	—	1.5	—	2.75	1.5	—	1.5	—	1.5	
V_O = 7.5 or 1.5		8	—	2.4	—	2.4	—	3.65	2.4	—	2.4	—	2.4	
V_O = 0.5 or 2.5	V_{IH}	3	2.1	—	2.1	—	2.1	1.65	—	2.1	—	2.1	—	
V_O = 0.5 or 4.5		5	3.5	—	3.5	—	3.5	2.75	—	3.5	—	3.5	—	
V_O = 1.5 or 7.5		8	5.6	—	5.6	—	5.6	4.45	—	5.6	—	5.6	—	
Output Current V_{OH} = 2.7	I_{OH}	3	−1.6	—	−1.6	—	−1.4	−2.0	—	−0.8	—	−0.8	—	
V_{OH} = 4.6		5	−2.4	—	−2.4	—	−2.0	−2.8	—	−1.6	—	−1.6	—	
V_{OH} = 7.5		8	−4.8	—	−4.8	—	−3.6	−4.6	—	−2.8	—	−2.8	—	
V_{OL} = 0.3	I_{OL}	3	1.6	—	1.6	—	1.4	2.0	—	0.8	—	0.8	—	
V_{OL} = 0.4		5	2.4	—	2.4	—	2.0	2.8	—	1.6	—	1.6	—	
V_{OL} = 0.5		8	4.8	—	4.8	—	3.6	4.6	—	2.8	—	2.8	—	
Input Current f_{in}, OSC_{in}	I_{in}	8	—	±50	—	±50	—	±10	±25	—	±22	—	±22	μAdc
Other Inputs	I_{IH}	8	—	±0.3	—	±0.3	—	±.00001	±0.1	—	±1.0	—	±1.0	
Input Capacitance	C_{in}	3–8	—	10	—	10	—	6	10	—	10	—	10	pF
Output Capacitance	C_{out}	3–8	—	10	—	10	—	6	10	—	10	—	10	pF
3-State Leakage Current PD_{out}	I_L	8	—	±0.1	—	±0.1	—	±0.0001	±0.1	—	±10	—	±10	μAdc
Quiescent Current (Static)	I_{DD}	8	—	150	—	150	—	40	150	—	150	—	150	μAdc

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SWITCHING CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Units
Output Rise and Fall Time All Outputs	t_{TLH} t_{THL}	3 5 8	— — —	15 10 5	20 15 10	ns
Setup Time Data to Clock	t_{SU}	3 5 8	50 40 30	20 10 9	— — —	ns
Clock to Enable	t_{SU}	3 5 8	100 50 30	30 15 10	— — —	ns
Hold Time Clock to Data	t_H	3 5 8	10 15 20	5 8 10	— — —	ns
Recovery Time Enable to Clock	t_{REC}	3 5 8	10 15 20	−2 −3 −3	— — —	ns
Output Pulse Width PHIR, PHIV with f_R in Phase with f_V	t_{WO}	3 5 8	70 40 30	250 150 100	500 300 200	ns
Input Rise and Fall Times OSC_{in}, f_{in}	t_{TLH} t_{THL}	3 5 8	— — —	10 5 2	5 2 0.5	μs
Input Pulse Width Clock, Enable	t_W	3 5 8	60 50 40	30 25 20	— — —	ns

(TA = −55°C to +125°C, C_L = 50 pF)

FREQUENCY CHARACTERISTICS

Characteristic	Symbol	Division Ratio	V_{DD}	−55°C to 125°C Max	Typical	−40°C to 85°C Max	Units
Operating Frequency f_{in} OSC_{In} Input=SQ Wave V_{DD}−V_{SS} or Sinewave 500mVP-P	f_{max}	≥10	3 5 8	10 15 20	28 30 30	11 17 21	MHz
		3	3 5 8	3.5 5 8	12 16 24	4 6 9	

PIN DESCRIPTIONS

RA0, RA1, RA2 (Pins 18, 1, and 2) – These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below.

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	16
0	0	1	512
0	1	0	1024
0	1	1	2048
1	0	0	3668
1	0	1	4096
1	1	0	6144
1	1	1	8192

ΦR, ΦV (Pins 3 and 4) – These phase detector outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ΦV pulsing low. ΦR remains essentially high.

If the frequency of f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ΦR pulsing low. ΦV remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, both ΦV and ΦR remain high except for a small minimum time period when both pulse low in phase.

V_{DD} (Pin 5) – Positive power supply.

PD_{out} (Pin 6) – Three state output of phase detector for use as loop error signal. Double-ended outputs are also available for this purpose (see ΦV and ΦR).

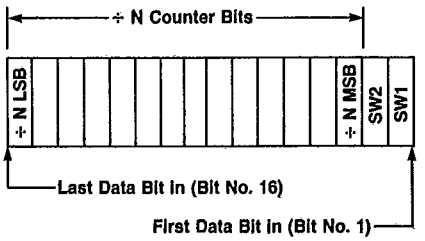
Frequency $f_V > f_R$ or f_V leading: negative pulses
Frequency $f_V < f_R$ or f_V lagging: positive pulses
Frequency $f_V = f_R$ and phase coincidence: High-impedance state.

V_{SS} (Pin 7) – Circuit ground.

LD (Pin 8) – Lock detector signal. High level when loop is locked (f_R, f_V same phase and frequency). Pulses low when loop is out of lock.

f_{in} (Pin 9) – Input to the ÷N portion of the synthesizer, f_{in} is typically derived from the loop VCO, and is AC-coupled into Pin 9. For larger amplitude signals (standard CMOS logic levels) DC coupling may be used.

CLOCK, DATA (Pins 10 and 11) – Shift register clock and data input. Each low-to-high transition clocks one bit into the on-chip 16-bit shift register. The data is presented on the DATA input at the time of the positive clock transition the DATA input provides programming information for the 14-bit ÷N counter and the two switch signals SW1 and SW2. The entry format is as follows:



ENABLE (Pin 12) – When high (1) transfers contents of the shift register into the latches, and to the programmable counter inputs and the switch outputs SW1 and SW2. When low (0) inhibits the above action and allows changes to be made in the shift register data without affecting the counter programming and switch outputs. An on-chip- pull-up establishes a continuously high level for ENABLE when no external signal is applied to Pin 12.

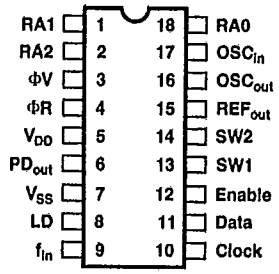
SW1, SW2 (Pins 13 and 14) – SW1 and SW2 provide latched open drain outputs corresponding to data bits numbers one and two. These will typically be used for band switch functions. A logic one will cause the output to assume a high-impedance state, while a logic zero will cause an output logic zero.

REF_{out} (Pin 15) – Buffered output of on-chip reference oscillator or externally provided reference-input signal.

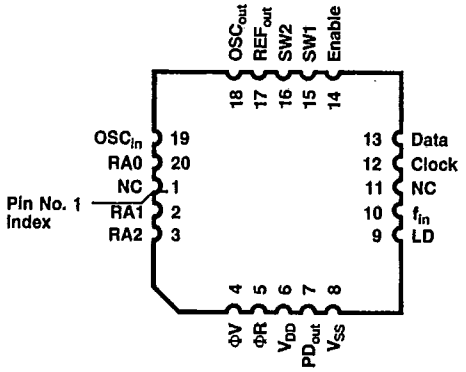
OSC_{out}, OSC_{in} (Pins 16 and 17) – These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency-setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally generated reference signal. This signal will typically be AC coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

CONNECTION DIAGRAMS

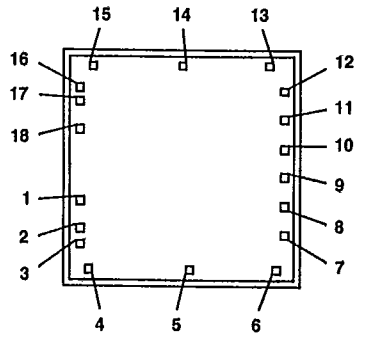
DUAL-IN-LINE PACKAGES



CHIP CARRIER



DIE LAYOUT



NOTE: Pin numbers correspond to DIP pin-out.

ORDERING INFORMATION

VALID COMBINATIONS:

IMI145155018**PB**
IMI145155020**QB**
IMI145155018**XB**
IMI145155018**ST**
IMI145155018**SK**
IMI145155020**LT**
IMI145155020**LK**
IMI145155000**DG**
IMI145155000**DQ**

For detailed ordering information see page 2.